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EXAMINER

TRAN, NHAN T

ART UNIT PAPER NUMBER

2615

DATE MAILED: 01/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/359,056

Applicant(s)

MANSOORIAN, BARMAK

Examiner

Nhan T. Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 August 2004.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 14 and 17 is/are allowed.
6) ☒ Claim(s) 1-13, 15 and 16 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/6/2004 have been fully considered but they are not persuasive.

Regarding claim 1, the Applicant argues that:

(1) Nothing in Pain teaches or suggests that the digital output 110 includes a "current mode output," or that a receiving portion on the other end of digital output 110 "receiv[es] said current mode output" (Remarks, page 7);

(2) The motivation to minimize noises is not based on anything that is disclosed in the references or to what the references relate (Remarks, page 8);

(3) The Office Action points to nothing in either Pain or Pickering that would suggest a need to variably control (variable load) the impedance of the devices, and that the combination of Pain, Pickering and Gabara is improper (Remarks, page 9).

In response, the Examiner respectfully clarifies the Office Action:

(1) Pain clearly discloses that the ADC array is a current mode ADC (col. 7, lines 15-16). The output of the ADC is shown as a differential non-linearity output in a 12-bit current mode (see Figs. 12B and col. 3, lines 10-14). Although Pain does not clearly disclose an image receiving portion for receiving the image data output from the ADC array, Figs. 1A-1C imply another device (i.e., another chip) to be connected to the output of the ADC array in order to form a complete imaging system. Since the output of the ADC array is a current mode output, a compatible current mode input at the receiving portion **must** be implemented for the system to

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function properly. Therefore, one skilled in the art would recognize that an image receiving portion would be implemented following the output of the ADC array without explicit disclosure of such a portion in the drawings in Pain.

(2) The Examiner has already provided the motivation taught by Pickering to minimize the effects of common-mode noise and reflection noise using CMOS differential driver in a current mode for driving and matching impedance of transmission line (Pickering, Fig. 1; col. 2, lines 17-26, 45-50). The teaching of Pickering relates to a high-speed chip-to-chip data interface in a digital communication system (Pickering, col. 1, lines 5-7) implemented by using CMOS differential output driver in current mode which compensates the deficiencies in Pain for such teachings for digital data interface between different portions of an imaging system. Since both Pain and Pickering deal with digital data processing using CMOS technology and Pickering teaches what Pain is silent about, these references are substantially related to each other for a reasonable combination as analyzed above and in the previous Office Action.

(3) Although Pain and Pickering do not teach a variable load to adjust the impedance of an active impedance matching device, this teaching is taught by Gabara in col. 4, lines 35-41, wherein a clearly obvious design variation is described for using either passive impedance elements, such as resistors, or a plurality of active impedance elements such as MOSFET transistors in an impedance control module. Therefore, the obviousness is established based on the suggestion in Gabara. One skilled in the art would combine the teachings of Pain, Pickering and Gabara to enhance the imaging system with an active impedance matching device for an off-chip data interface in view of the above suggestions.

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Regarding claim 15, the Applicant asserts that no teaching, suggestion or motivation is provided in support of the Official Notice that the Examiner inserted in the Office Action.

In response, the Examiner respectfully submits that the active impedance matching device has been taught in the combination of Pain, Pickering and Gabara. The only thing that is not disclosed is adjusting bias current of a transistor in way that renders the input impedance relatively independent of an input current. However, the active impedance matching device is to control the impedance looking into the input and/or output of a transistor, which can be configured by adjusting bias current of a transistor in a well-known fashion so that input impedance is relatively independent of an input current. The Examiner has provided this well-known teaching of adjusting bias current to adjust the impedance (resistance) of a transistor in Saari (US 4,441,080), col. 2, lines 54-58. Thus, there is a conventional teaching to motivate any one skilled in the art to change the input impedance of a device by adjusting the bias current of the active impedance element (transistor) to render the input impedance relatively independent of an input current.

In view of the above, the Examiner believes that the interpretation of the present claimed limitations read on the cited references for at least the reasons discussed above and as stated in the following Office Action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-13, 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Pickering et al (US 5,050,194) and in further view of Gabara (US 5,739,714).

Regarding claim 1, Pain discloses an image sensor, comprising:
an image acquisition portion (100, 112) as shown in figs. 1A-1C, col. 3, lines 52-63;
an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current mode output (see fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output. Since the ADC array is configured with CMOS current driving mode, the impedance must exist at the ADC array output and throughout transmission line(s).

Pain's disclosure of digital output of the ADC array (figs. 1A-1C) implies another separate portion (i.e., another chip) to be connected thereto for receiving digital image data output from the ADC array. The implied separate portion represents "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs, and said image receiving portion receiving current mode output" in order to form a complete imaging system of CMOS compatible applications (see col. 2, lines 5-7 for a consistent CMOS compatible).

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Therefore, it would have been obvious to one of ordinary skill in the art to recognize another chip connected to the digital output from the image processing portion (ADC array 118) as an image receiving portion which would be also configured in CMOS having input characteristics being compatible with the digital output of the image processing portion to function in a complete imaging system.

Pain does not explicitly disclose the CMOS outputs being differential outputs and an active impedance matching device being adapted to match said output impedance of said image processing portion to said input impedance of said image receiving portion.

As taught by Pickering, differential output driver (1) and differential input driver (8) are implemented in CMOS technology for transmitting and receiving off-chip data, and matching impedances of the drivers with transmission line is also performed at the output and input of the drivers to minimize common mode noise and noise caused by reflections (see Fig. 1; col. 2, lines 17-26, 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art to combine Pain with the teaching of Pickering for differential output and input drivers of the devices using CMOS technology with a corresponding impedance matching device to transmit and receive off-chip data thereby common mode noise and noise caused by reflections would be minimized.

Although Pickering teaches the CMOS differential output and input drivers and the corresponding **passive** impedance matching device using a passive termination circuit (resistors), Pickering fails to teach an **active** impedance matching device. However, the active impedance matching device using an active termination circuit implemented with transistors is an obvious

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variant over the passive one in circuit design for variably controlling impedance as taught by Gabara in col. 4, lines 35-41.

Therefore, it would have been obvious to one of ordinary skill in the art to implement the impedance matching device using active impedance elements such as transistors to variably control (variable load) the impedance of the devices in the combination of Pain and Pickering as an obvious circuit design variation over the passive one.

Regarding claim 2, the image processing portion includes a portion with a CMOS output (3) as shown by Pickering in Fig. 1.

Regarding claims 3 & 6, Pickering also discloses that impedance matching circuits (termination circuits 6) are implemented at both ends (see Fig. 1; col. 2, lines 59-61). It is noted that the analysis in claim 1 for active termination circuit is also applied in these claims.

Regarding claim 4, Pickering discloses a current source (shown in block 3 of Fig. 1) used to bias the transistors wherein the corresponding impedance inherently exists at the output of each transistor in response to the bias current.

Regarding claim 5, the output impedance is matched to input impedance of the image receiving circuit as analyzed in claim 1.

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Regarding claim 7, Pickering shows differential input buffer (8) at the receiver (7). It is noted that the same analysis in claim 4 is applied to claim 7 for the input impedance.

Regarding claim 8, the input impedance is matched to output impedance of the image receiving circuit as analyzed in claim 1.

Regarding claim 9, the claimed limitations are analyzed with respect to claims 3 & 6.

Regarding claim 10, the claimed limitations are analyzed with respect to claims 4 & 7.

Regarding claim 11, the claimed limitations are analyzed with respect to claims 5 & 8.

Regarding claim 12, Pickering shows a current source used for biasing the transistors in the differential buffer 3 (Fig. 1). Pickering does not teach that the current source is a current mirror part. However, an Official Notice is taken that the current source can be configured by current mirror in CMOS applications.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize an alternative configuration for the current source in Pickering would be a well known current mirror.

Regarding claim 13, Pain discloses the image acquisition circuit being an active pixel sensor (APS 300) with a photosensor (photogate 310), an in-pixel buffer (floating diffusion 330,

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transistor 360), and in-pixel select transistor (vertical select 370) (see fig. 3A; col. 6, lines 25-49).

Regarding claim 15, Pain, Pickering and Gabara disclose all limitations of claim 15 except for explicitly disclosing the limitation of matching impedances by adjusting bias current through at least one biased device in a way that renders the input impedance relatively independent of an input current. Pickering and Gabara teach passive or active termination circuit connected at both transmitter and receiver ends to match impedances as analyzed in claim 1. An Official Notice is further taken that the active impedance transistors can provide variable termination resistance (variable load) by changing bias current of the transistors.

Therefore, it would have been obvious to one of ordinary skill in the art to adjust bias current of the active impedance transistors in a conventional fashion so that variable impedance control between the transmitter and the receiver would be realized independent of an input current

Regarding claim 16, the claimed limitations are analyzed with respect to claim 1.

Allowable Subject Matter

3. Claims 14 & 17 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

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The prior art of record fails to teach or fairly suggest the *combination of all limitations* required in each of claims 14 and 17, including the limitation of the image acquisition portion and the image processing portion operates at substantially zero voltage.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.



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